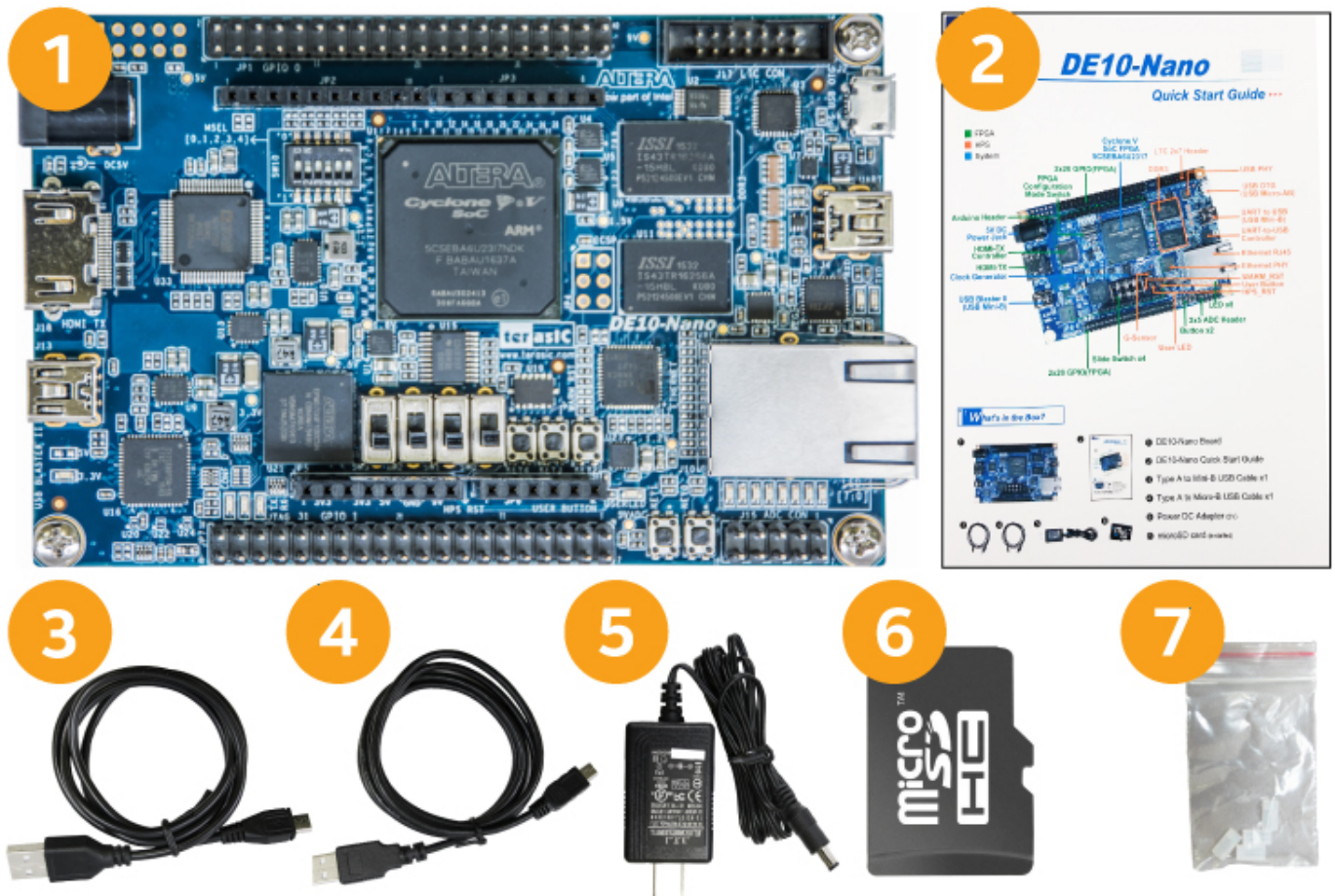


Introduction to the Terasic DE10-Nano

The Terasic DE10-Nano development board, based on an Intel® SoC FPGA, provides a reconfigurable hardware design platform for makers, IoT developers and educators. Featuring two GPIO expansion headers, an Arduino* header, high-speed DDR3 memory, an HDMI* port and ethernet networking, the board provides a robust and feature rich platform to create many exciting IoT applications.

Developers and makers are invited to discover the performance of a low-power embedded processor integrated with the flexibility of programmable logic. Divided into two distinct parts, the Intel® Cyclone® FPGA SoC device is made of a hard processor system (HPS) and a Field Programmable Gate Array (FPGA). While the HPS is a general purpose processor (based on a dual-core ARM Cortex-A9* processor), the FPGA is a parallel processing engine on which you can create custom hardware to accelerate fixed function algorithms or for extending the I/O capabilities of the device.

Terasic DE10-Nano Kit Contents



The Terasic DE10-Nano kit should come with 7 items:

- Terasic DE10-Nano Board
- Quick Start Guide
- Type A to Micro-B USB Cable
- Type A to Mini-B USB Cable
- 5V (2A) power supply
- microSD Card
- A bag of 4 silicon foot stands

The Altera Cyclone V SE 5CSEBA6U23I7

The Altera Cyclone V SE 5CSEBA6U23I7 is a high-performance System-on-Chip (SoC) FPGA designed for low-power, cost-sensitive embedded applications. It integrates a dual-core ARM Cortex-A9 MPCore processor with CoreSight, operating at up to 800 MHz, alongside an FPGA fabric featuring 110,000 logic elements (LEs). Built on TSMC's 28 nm low-power process technology, it offers up to 13.59 Mb of embedded memory through M10K and MLAB blocks, and supports advanced I/O capabilities, including PCIe, USB, and DDR3 memory interfaces. The device is housed in a 672-pin UBGA package (23x23 mm) and provides flexible programmable interconnects for customized designs, making it ideal for applications in digital signal processing, hardware acceleration, and embedded systems requiring robust performance and energy efficiency.

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